Debugging

Stellaris microcontrollers support programming and debugging using either JTAG or SWD. JTAG uses the signals TCK, TMS, TDI, and TDO. SWD requires fewer signals (SWCLK, SWDIO, and, optionally, SWO for trace). The debugger determines which debug protocol is used.

调试

Stellaris系列为控制器支持JTAG或SWD进行编程和调试。JTAG使用信号引脚TCK、TMS、TDI和TDO。SWD需要的信号引脚较少(SWCLK, SWDIO, and, optionally, SWO for trace)。由调试器决定使用哪种调试协议。

Debugging Modes

The LM3S8962 evaluation board supports a range of hardware debugging configurations. Table 2-1 summarizes these configurations.

调试模式

LM3S8962评估板支持一些硬件调试配置，表2-1总结了这些配置。

Table 2-1. Stellaris LM3S8962 Evaluation Board Hardware Debugging Configurations
表2-1. Stellaris LM3S8962评估板硬件调试配置

Mode 模式	Debug Function 调试功能	Use 用途	Selected by 选择
1	Internal ICDI 内部ICDI	Debug on-board LM3S8962 microcontroller over USB interface. 通过USB接口调试板上LM3S8962微控制器	Default mode 默认模式
2	ICDI out to JTAG/SWD header ICDI从JTAG/SWD接口输出	The EVB is used as a USB to SWD/JTAG interface to an external target. 评估板作为一个USB的SWD/JTAG接口用于调试外部目标芯片	Connecting to an external target and starting debug software. The red Debug Out LED will be ON. 连接一个外部目标芯片并启动调试软件，红色调式输出LED灯将会亮起
3	In from JTAG/SWD header 从JTAG/SWD接口输入	For users who prefer an external debug interface (ULINK, JLINK, etc.) with the EVB. 根据用户喜好对评估板使用一个外部调试接口(ULINK, JLINK等)	Connecting an external debugger to the JTAG/SWD header. 连接一个外部调式器到JTAG/SWD接口

Modes 2 and 3 automatically detect the presence of an external debug cable. When the debugger software is connected to the EVB's USB controller, the EVB automatically selects Mode 2 and illuminates the red Debug Out LED.

模式2和3自动检测外部调试电缆的存在。当调试器软件连接到评估板的USB控制器，评估板自动选择模式2并点亮红色调试输出LED。可以参考：
http://www.ourdev.cn/bbs/bbs_content.jsp?bbs_sn=3828076&bbs_page_no=8&bbs_id=3011

Debug In Considerations

Debug Mode 3 supports evaluation board debugging using an external debug interface. Mode 3 is automatically selected when a device such as a Segger J-Link or Keil ULINK is connected. Boards marked Revision B or later automatically configure pin 1 to be a 3.3-V reference, if an external debugger is connected. To determine the revision of your board, locate the product number on the bottom of the board; for example, EK-LM3S8962-B. The last character of the product number identifies the board revision.

A configuration or board-level change may be necessary when using an external debug interface with revision A of this evaluation board. Because the evaluation board supports both debug out and debug in modes, pin 1 of the 20-pin JTAG/SWD header is, by default, not connected to +3.3 V. Consequently, devices requiring a voltage on pin 1 to power their line buffers may not work.

Two solutions exist. Some debugger interfaces (such as ULINK) have an internal power jumper that, in this case, should be set to internal +3.3 V power. Refer to debugger interface documentation for full details. However, if your debugger interface does not have a selectable power source, it may be necessary to install a 0-Ω resistor on the evaluation board to route power to pin 1. Refer to the schematics and board drawing in the appendix of this manual for the location of this resistor.

调试注意事项

模式3支持使用外部调试接口调试评估板。当一个设备例如Segger J-Link或Keil ULINK连接到评估板上时自动选择模式3。

如果连接了一个外部调试接口，评估板上有记号修正版B或更迟的版本自动配置JTAG/SWD接口的PIN1为3.3V参考。请确定你的评估板的修正号，位于评估板底部的产品编号。例如EK-LM3S8962-B。产品编号的最后一个数字作为评估板的修正号。

当对修正版A的评估板使用外部调试接口时，进行配置或线路板级变化是必需的。因为评估板支持调试输出和调试输入模式，JTAG/SWD接口的PIN1默认没有连接到+3.3V。因此，对于必需通过PIN1为线缓冲器提供电压的设备可能不能工作。

有两种解决方案。一些调试接口（例如ULINK）有一个内部电源跳线，在这种情况下，必需连接到内部+3.3V电源。细节请参考调试接口文档。然而，如果你的调试接口的电源支持不可选，它可能需要通过0欧姆的电阻连接评估板的电源到PIN1。请参考本手册附录的电路图和电路板布局来确定这个电阻的位置。可以参考：http://www.ourdev.cn/bbs/bbs_content_all.jsp?bbs_sn=3827239

USB Device Controller Functions
USB设备控制器功能

USB Overview
An FT2232 device from Future Technology Devices International Ltd. manages USB-to-serial conversion. The FT2232 is factory-configured by Luminary Micro to implement a JTAG/SWD port (synchronous serial) on channel A and a Virtual COM Port (VCP) on channel B. This feature allows two simultaneous communications links between the host computer and the target device using a single USB cable. Separate Windows drivers for each function are provided on the Documentation and Software CD.
A small serial EEPROM holds the FT2232 configuration data. The EEPROM is not accessible by the LM3S8962 microcontroller.
For full details on FT2232 operation, go to www.ftdichip.com.

USB概述
使用Future Technology Devices International Ltd.的FT2232实现USB-to-serial的转换。FT2232通过Luminary Micro出厂配置为在通道A实现一个JTAG/SWD端口（同步串行）和在通道B实现一个虚拟串行通讯端口（VCP）。此功能允许主机和目标设备之间通过一条USB电缆同时进行JTAG/SWD和VCP通讯。在Documentation and Software CD上为每个功能提供了Windows驱动软件。
一个小容量串行EEPROM用于保存FT2232配置数据。该EEPROM不允许通过LM3S8962微控制器进行访问。
有关FT2232的全部细节，请到www.ftdichip.com。

USB to JTAG/SWD
The FT2232 USB device performs JTAG/SWD serial operations under the control of the debugger. A CPLD (U6) multiplexes SWD and JTAG functions and, when working in SWD mode, provides direction control for the bidirectional data line. The CPLD also implements logic to select between the three debug modes. The internal or external target selection is determined by multiplexing `TCK/SWCLK` and asserting `TRST`.

USB转JTAG/SWD
FT2232 USB设备受调试器控制完成JTAG/SWD串行操作。CPLD（U6）提供多元的SWD和JTAG功能，当工作在SWD模式时，为双向数据线提供方向控制。CPLD也实现了三种调试模式之间的选择逻辑。内部和外部目标选择是由多路`TCK/SWCLK`和断言`TRST`决定的。

Virtual COM Port
The Virtual COM Port (VCP) allows Windows applications (such as HyperTerminal) to communicate with `UART0` on the LM3S8962 over USB. Once the FT2232 VCP driver is installed, Windows assigns a COM port number to the VCP channel.

虚拟串行通讯端口
虚拟串行通讯端口（VCP）允许Windows应用程序（例如：超级终端）通过USB与LM3S8962的`UART0`通讯。一旦安装了FT2232 VCP驱动，`Windows`将为VCP通道分配一个串行通讯端口。

Serial Wire Out

The evaluation board supports the Cortex-M3 serial-wire output (SWO) trace capabilities. Under debugger control, the CPLD can route the SWO datastream to the virtual communication port (VCP) transmit channel. The debugger can then decode and interpret the trace information received from the VCP. The normal VCP connection to `UART0` is interrupted when using SWO. Not all debuggers support SWO. Refer to the Stellaris LM3S3748 data sheet for additional information on the trace port interface unit (TPIU).

串行输出

评估板支持Cortex-M3串行输出（SWO）跟踪。在调试器控制下，CPLD可以发送SWO数据流到虚拟串行通讯端口（VCP）传输通道。调试器可以解码从VCP接收到的跟踪信息。当使用SWO时`UART0`与VCP的正常连接被中断。不是所有的调试器都支持SWO。查看Stellaris LM3S3748数据手册的附加信息跟踪端口接口单元（TPIU）。

ARM Target Pinout

In ICDI input and output mode, the Stellaris LM3S8962 Evaluation Kit supports ARM's standard 20-pin JTAG/SWD configuration. The same pin configuration can be used for debugging over serial-wire debug (SWD) and JTAG interfaces. The debugger software, running on the PC, determines which interface protocol is used.
The Stellaris target board should have a 2x10 0.1" pin header with signals as indicated in Table B-3. This applies to both an external Stellaris microcontroller target (Debug Output mode) and to external JTAG/SWD debuggers (Debug Input mode).

在ICDC输入和输出模式，Stellaris LM3S8962评估工具包支持ARM标准的20-pin JTAG/SWD配置。可以通过串行调试（SWD）接口和JTAG接口进行调试。PC运行的调试软件决定使用哪个接口协议。该Stellaris目标板有一个如表B-3所示的信号的2x10 0.1"接口。这适用于外部的Stellaris微控制器目标（调试输出模式）和外部JTAG/SWD调试（调试输入模式）。

Table B-3. 20-Pin JTAG/SWD Configuration

Function	Pin		Pin	Function
VCC (optional)	1		2	nc
nc	3		4	GND
TDI	5		6	GND
TMS	7		8	GND
TCK	9		10	GND
nc	11		12	GND
TDO	13		14	GND
nc	15		16	GND
nc	17		18	GND
nc	19		20	GND

ICDI does not control RST (device reset) or TRST (test reset) signals. Both reset functions are implemented as commands over JTAG/SWD, so these signals are not necessary.
It is recommended that connections be made to all GND pins; however, both targets and external debug interfaces must connect pin 18 and at least one other GND pin to GND.
ICDI不控制RST（设备复位）或TRST（测试复位）信号。这两种复位功能可以通过JTAG/SWD命令实现，因此这些信号不是必须的。
建议连接所有的GND引脚，然而，在目标调试和外部调试接口PIN 18和其他GND脚中的至少一个必须连接到GND。