天龙八步 之

Xilinx ISE 12.2 调用 Modelsim 进行行为仿真详解

最近闲来无事，整点东西，以飨各位。

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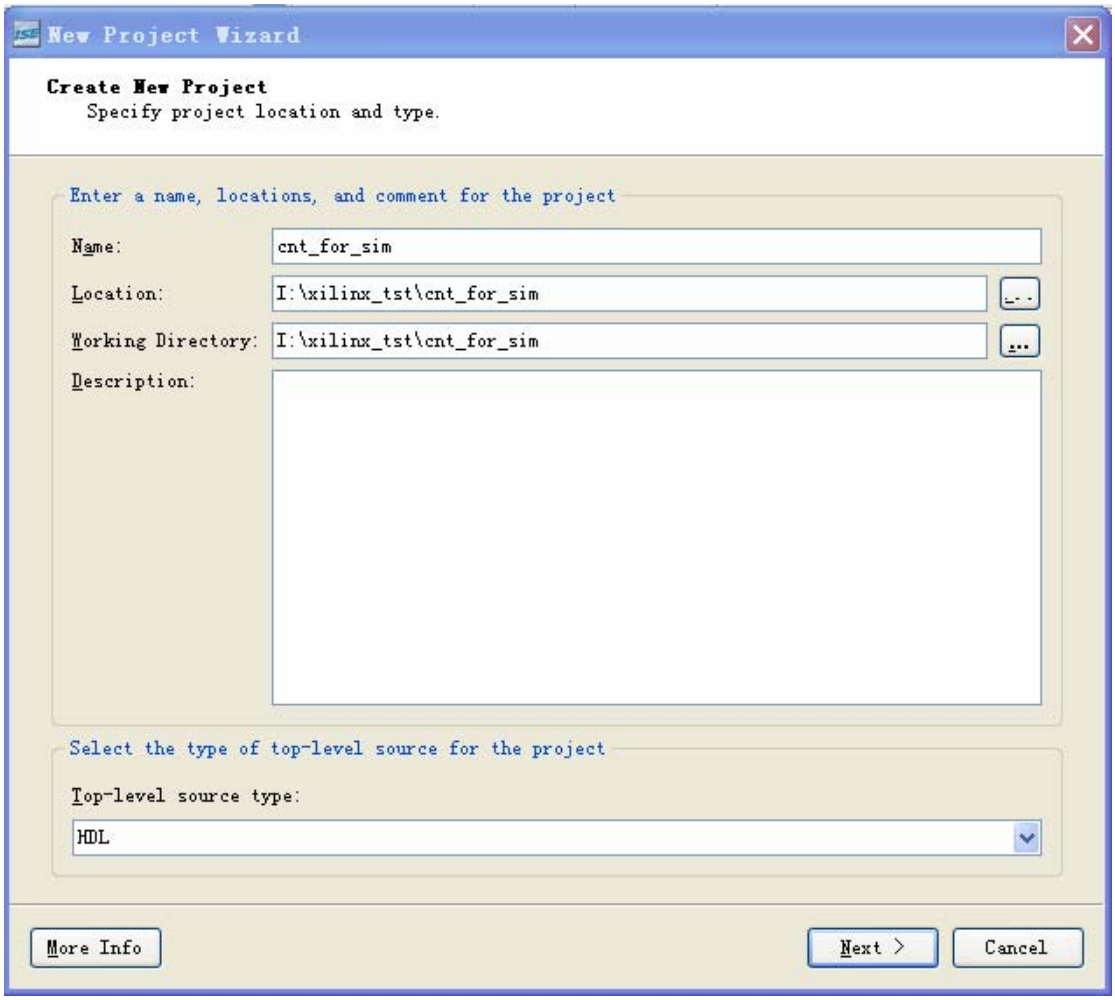
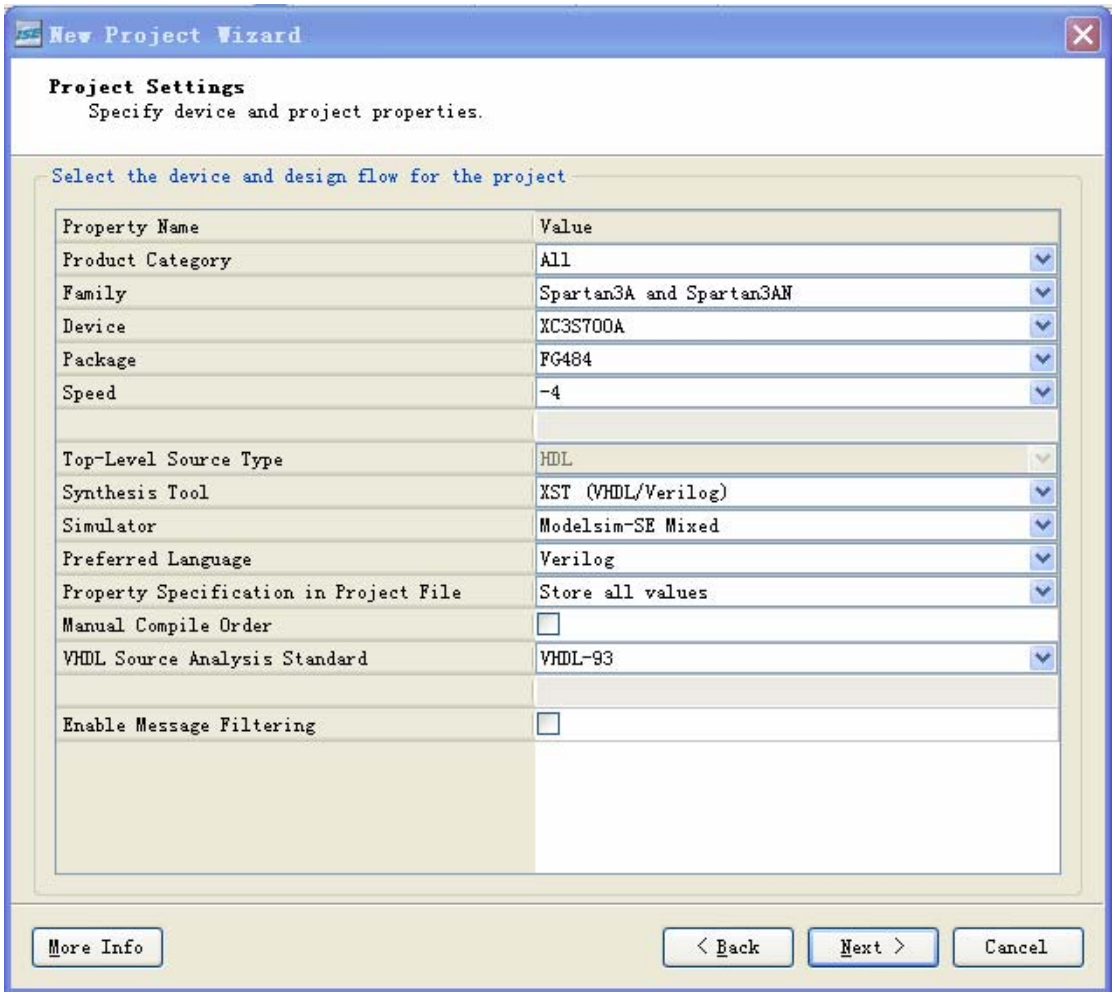
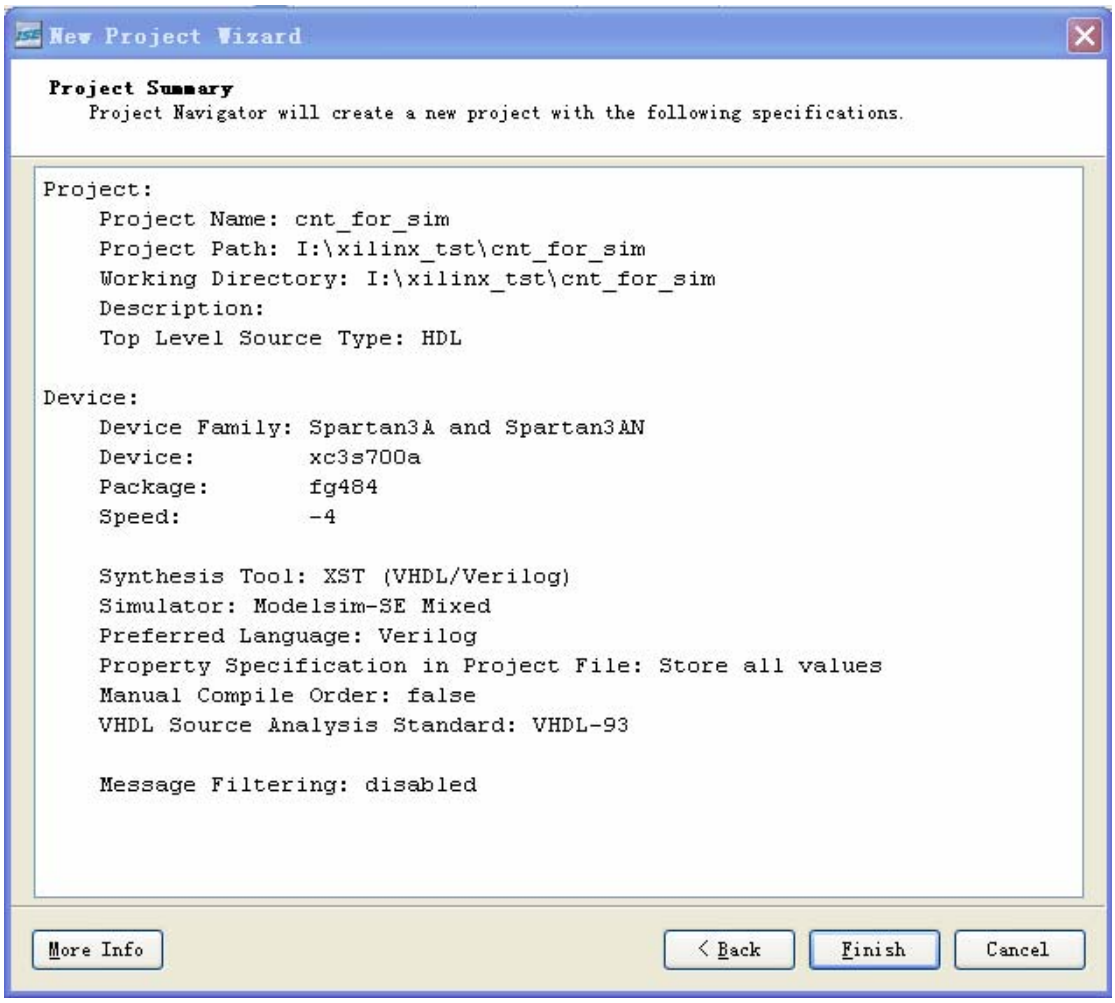
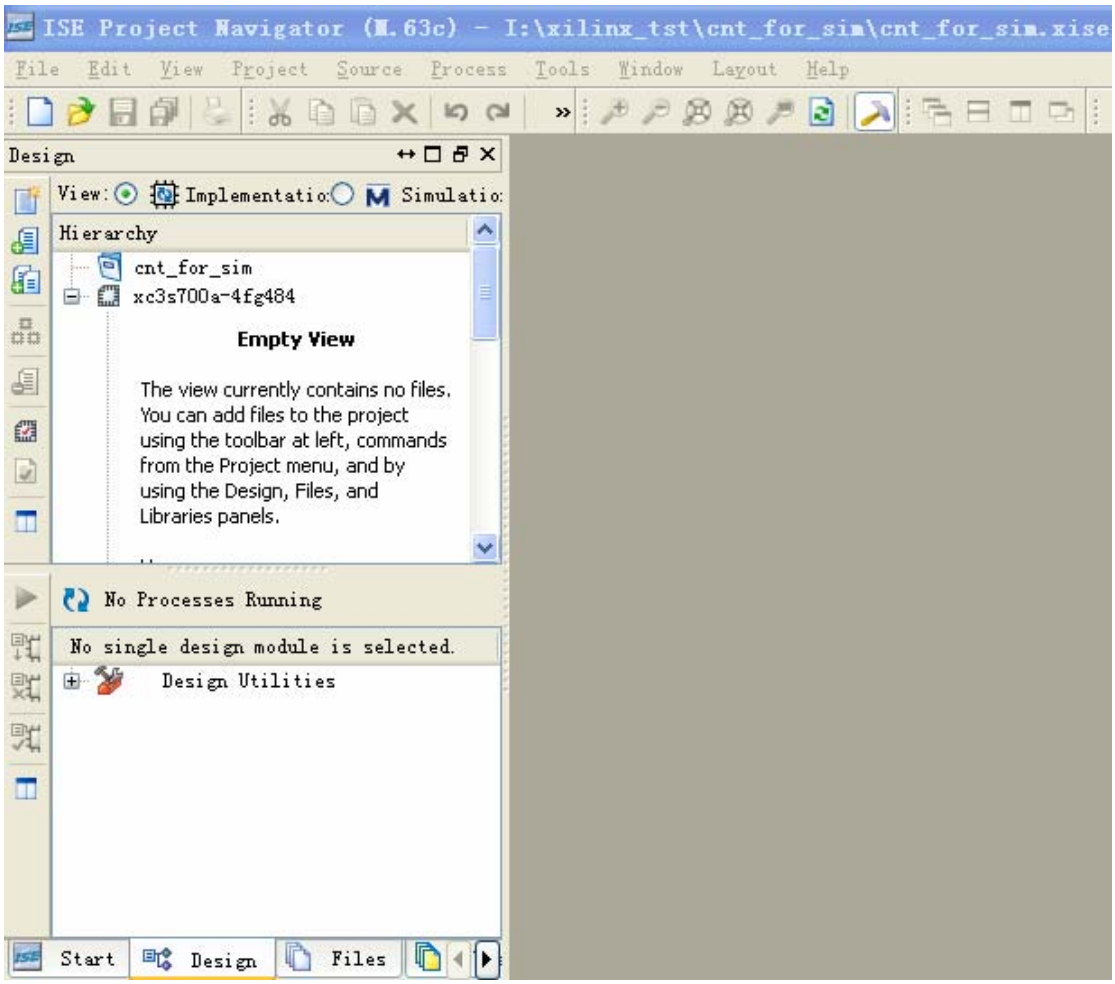
第一步：新建工程：

File->New Project 创建工程 cnt_for_sim，操作如下图。



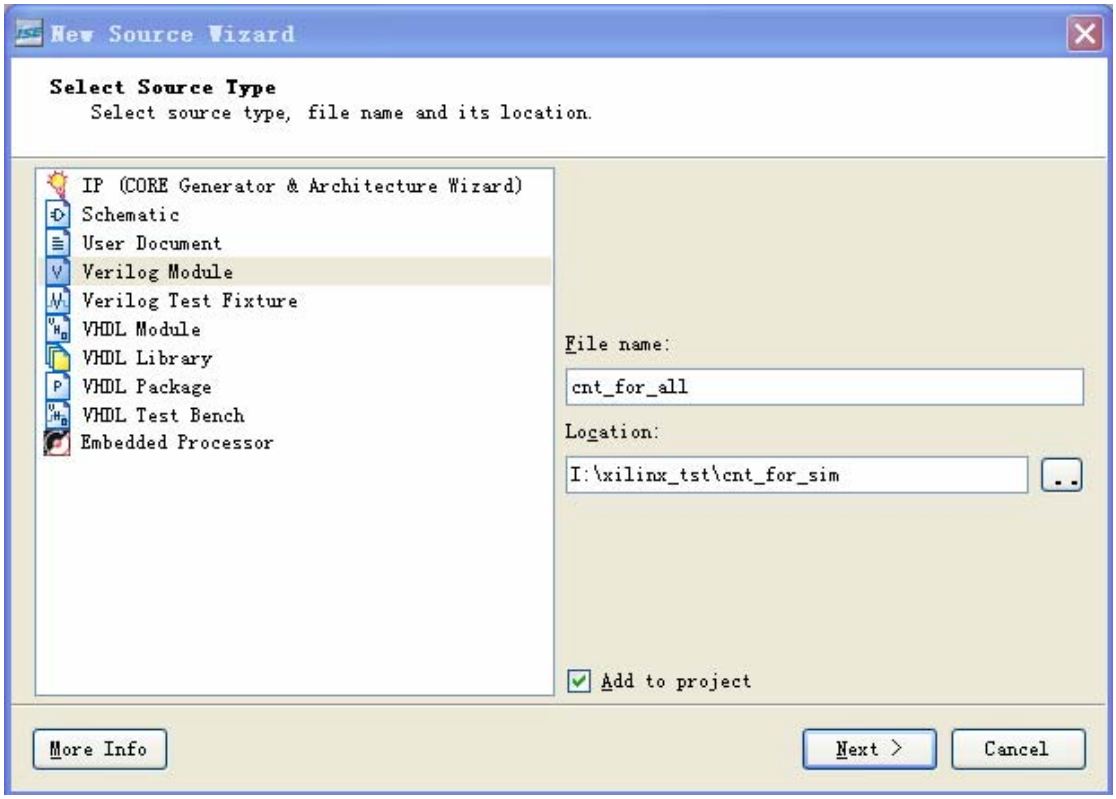

New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Product Category
All
Family
Spartan3A and Spartan3AN
Device
XC3S700A
Package
FG484
Speed
-4
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
Modelsim-SE Mixed
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
< Back
Next >
Cancel

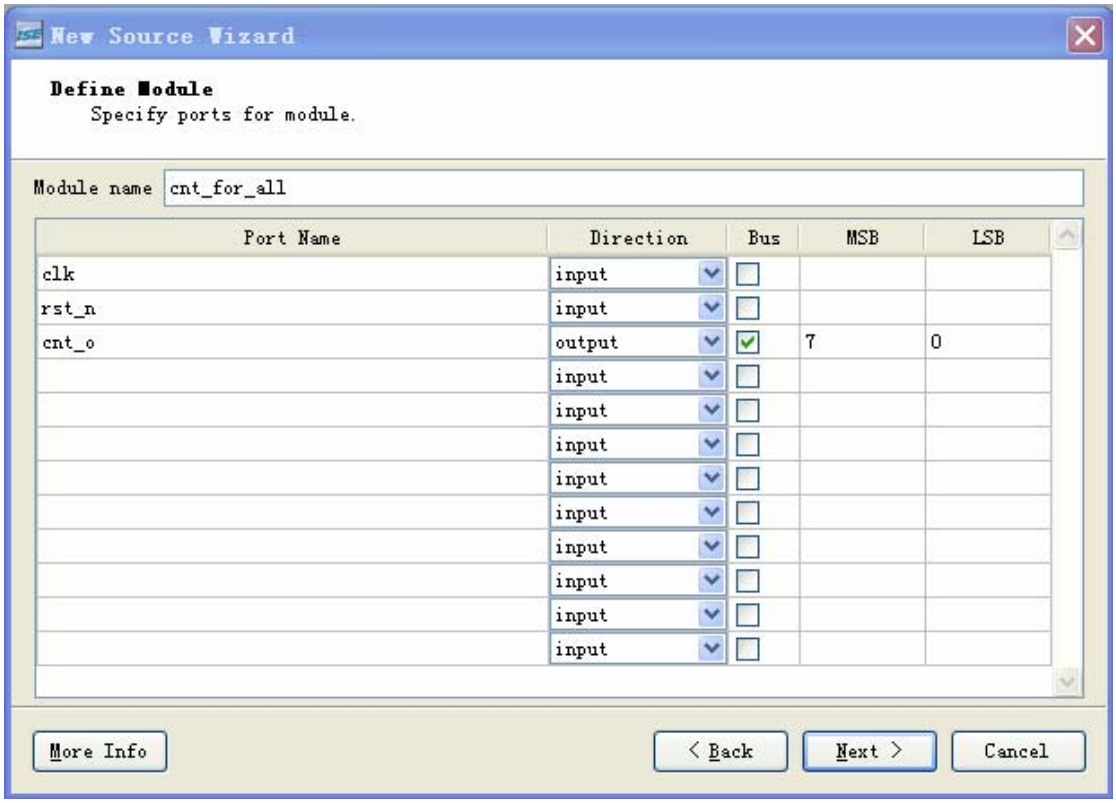

New Project Wizard
Project Summary
Project Navigator will create a new project with the following specifications.
Project:
Project Name: cnt_for_sim
Project Path: I:\xilinx_tst\cnt_for_sim
Working Directory: I:\xilinx_tst\cnt_for_sim
Description:
Top Level Source Type: HDL
Device:
Device Family: Spartan3A and Spartan3AN
Device: xc3s700a
Package: fg484
Speed: -4
Synthesis Tool: XST (VHDL/Verilog)
Simulator: Modelsim-SE Mixed
Preferred Language: Verilog
Property Specification in Project File: Store all values
Manual Compile Order: false
VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
More Info
< Back
Finish
Cancel

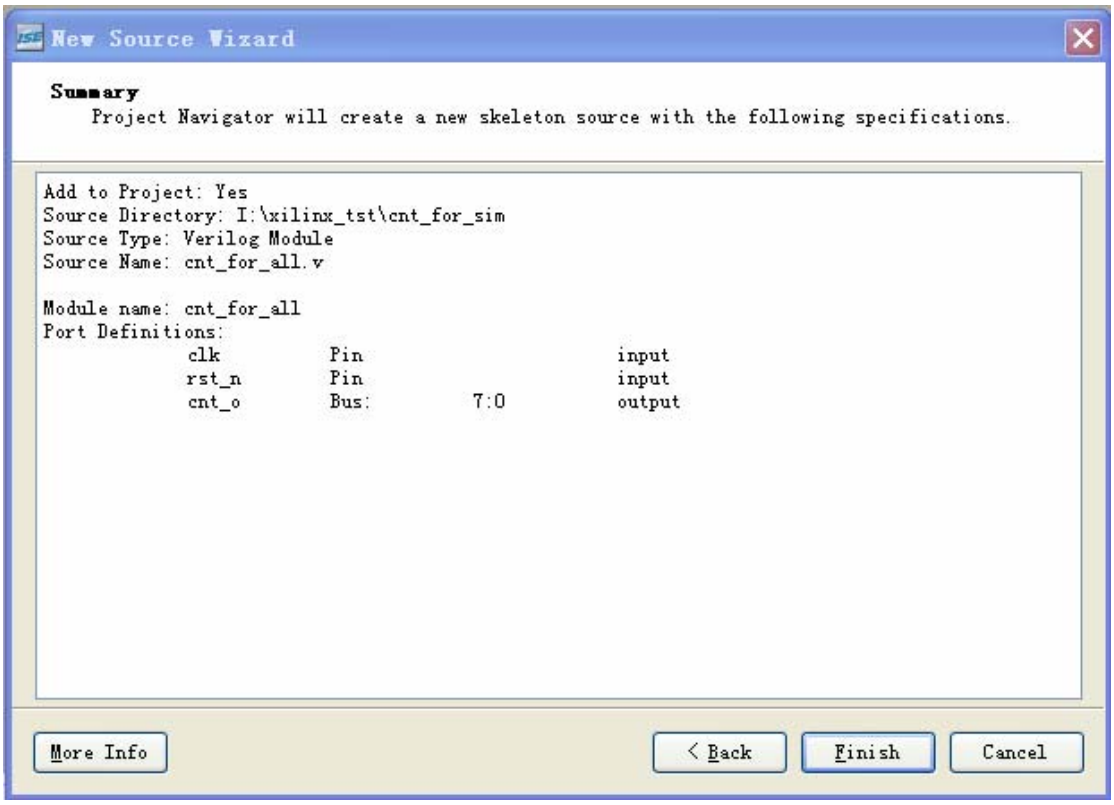


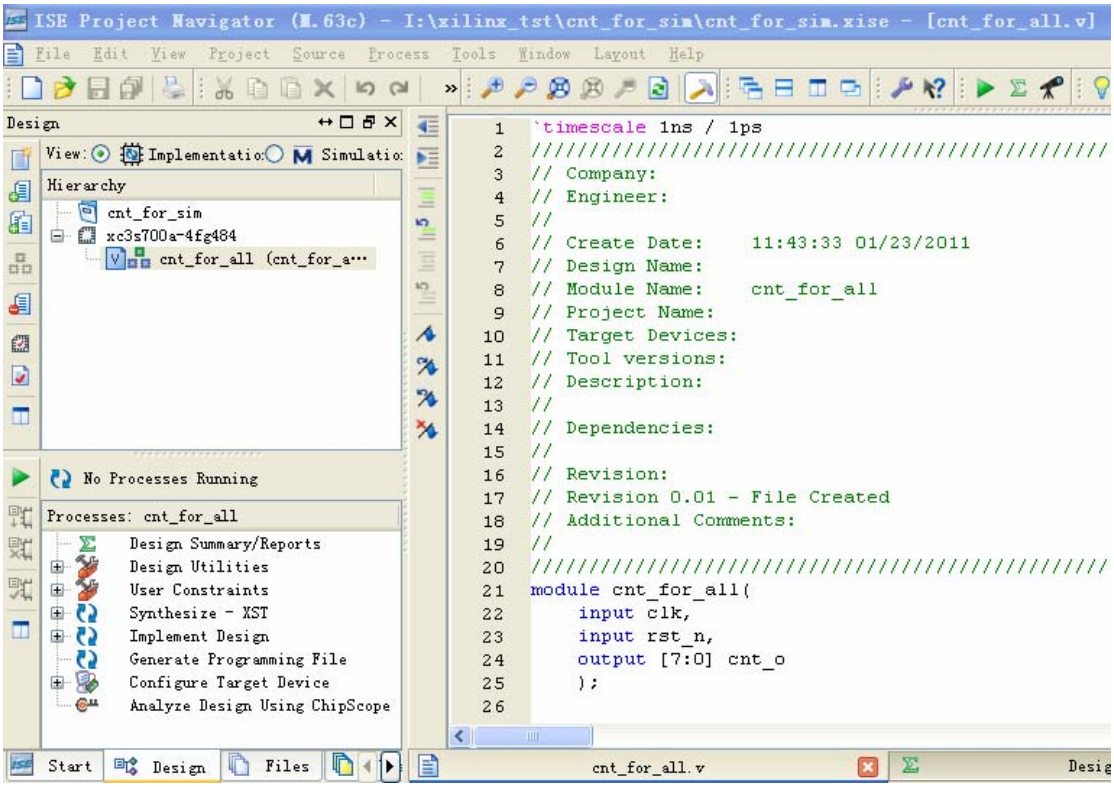
第二步：新建文件：

Project->New Source 创建文件 cnt_for_all.v，操作如下图。


New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
cnt_for_all
Location:
I:\xilinx_tst\cnt_for_sim
..
Add to project
More Info
Next >
Cancel


New Source Wizard
Define Module
Specify ports for module.
Module name
cnt_for_all
Port Name
Direction
Bus
MSB
LSB
clk
input
rst_n
input
cnt_o
output
7
0
More Info
< Back
Next >
Cancel





第三步：完善 cnt_for_all.v，如下：

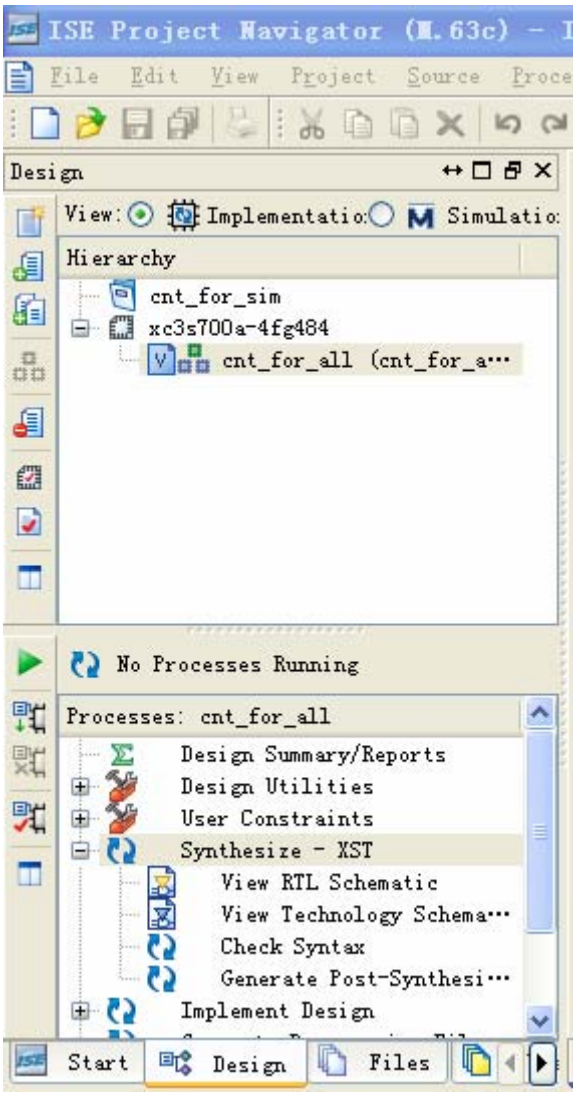
```
module cnt_for_all(
input clk,
input rst_n,
```

```
output [7:0] cnt_o
);
reg[7:0] cnt;
assign cnt_o = cnt;
always@(posedge clk or negedge rst_n)
begin
    if(!rst_n) cnt <= 8'd0;
    else cnt <= cnt + 1'd1;
end

endmodule
```

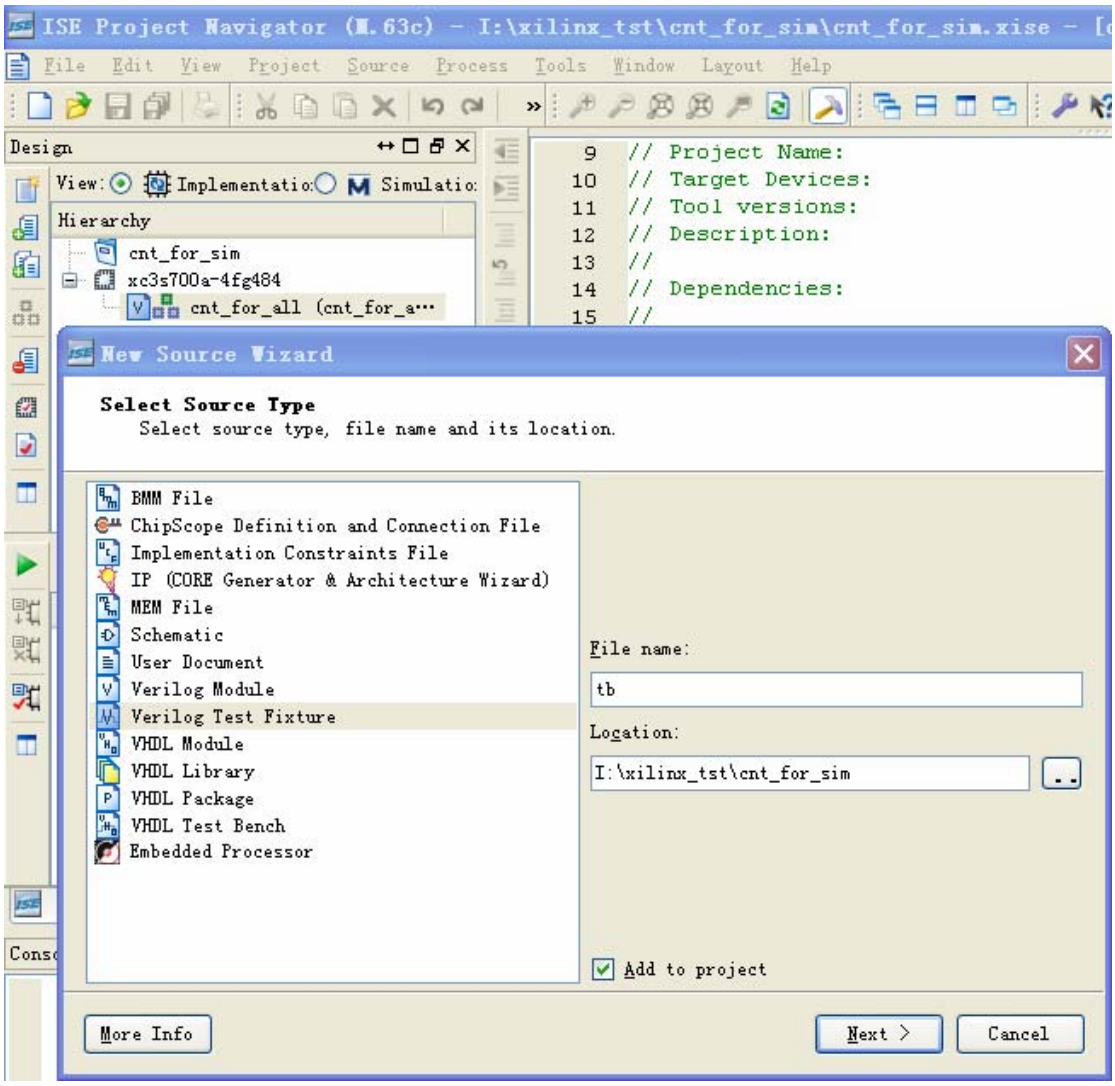
第四步：综合文件：

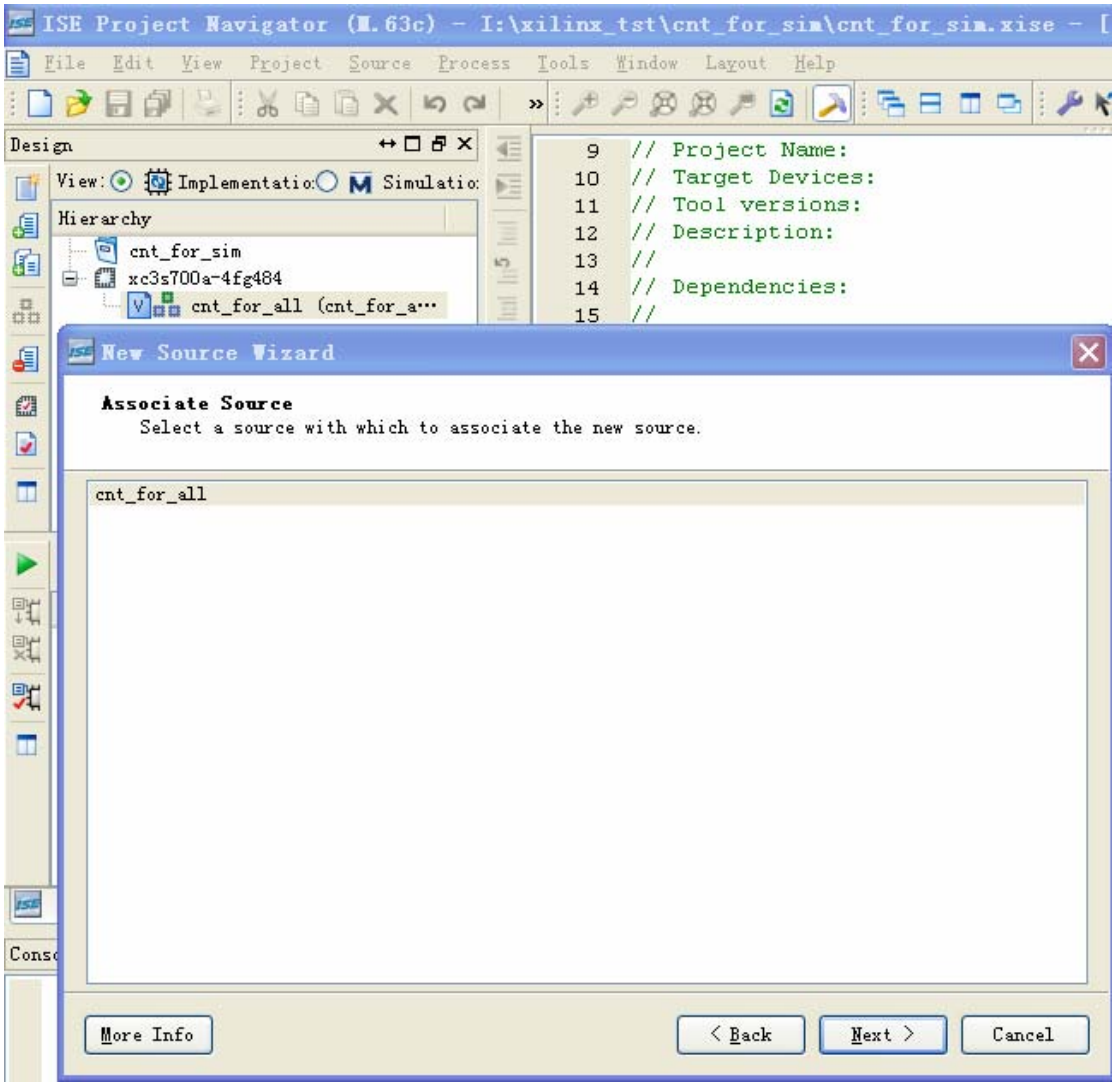
双击 Synthesize – XST，操作如下图。

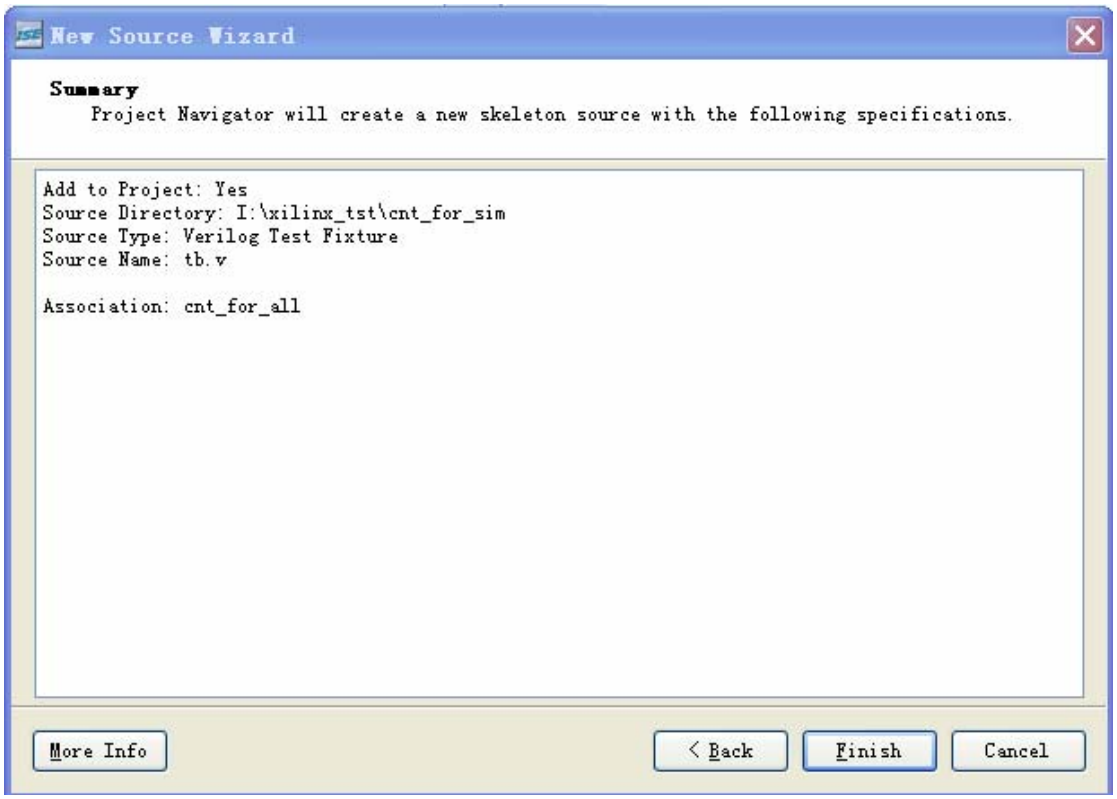


第五步：生成 verilog test bench 文件：

右击要仿真的文件 cnt_for_all.v，选择 New Source，操作如下图。

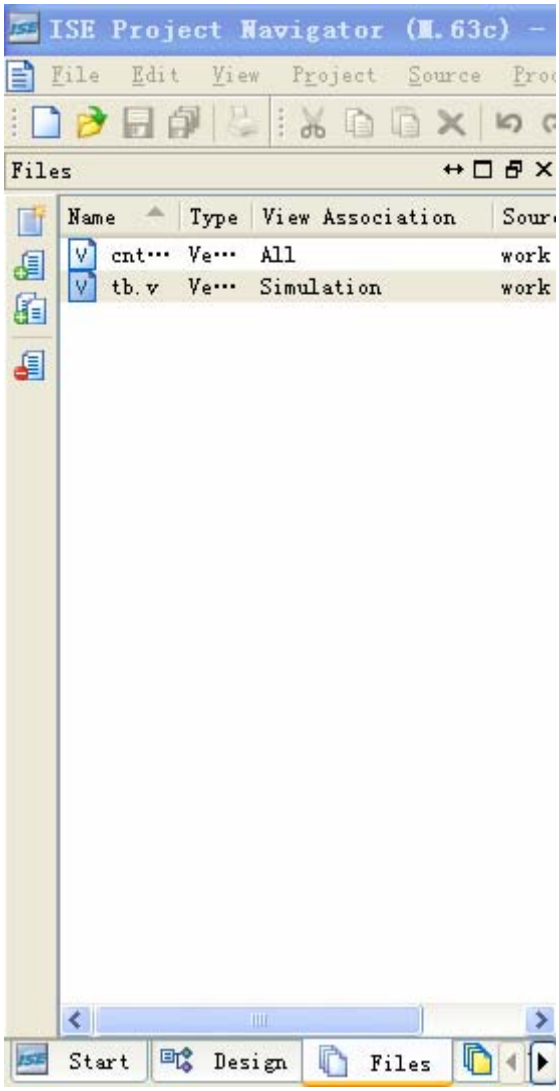

ISE Project Navigator (M.63c) - I:\xilinx_tst\cnt_for_sim\cnt_for_sim.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementatio Simulatio
Hierarchy
cnt_for_sim
xc3s700a-4fg484
cnt_for_all (cnt_for_a...
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
New Source Wizard
Select Source Type
Select source type, file name and its location.
BMM File
ChipScope Definition and Connection File
Implementation Constraints File
IP (CORE Generator & Architecture Wizard)
MEM File
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
tb
Location:
I:\xilinx_tst\cnt_for_sim
Add to project
More Info
Next >
Cancel


ISE Project Navigator (M.63c) - I:\xilinx_tst\cnt_for_sim\cnt_for_sim.xise - [
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementatio Simulatio
Hierarchy
cnt_for_sim
xc3s700a-4fg484
cnt_for_all (cnt_for_a…
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
New Source Wizard
Associate Source
Select a source with which to associate the new source.
cnt_for_all
More Info
< Back
Next >
Cancel



第六步：完善 tb.v 文件：

操作如下图：




```
module tb;
// Inputs
reg clk;
reg rst_n;

// Outputs
wire [7:0] cnt_o;

// Instantiate the Unit Under Test (UUT)
cnt_for_all uut (
        .clk(clk),
        .rst_n(rst_n),
        .cnt_o(cnt_o)
        );

initial begin
// Initialize Inputs
```

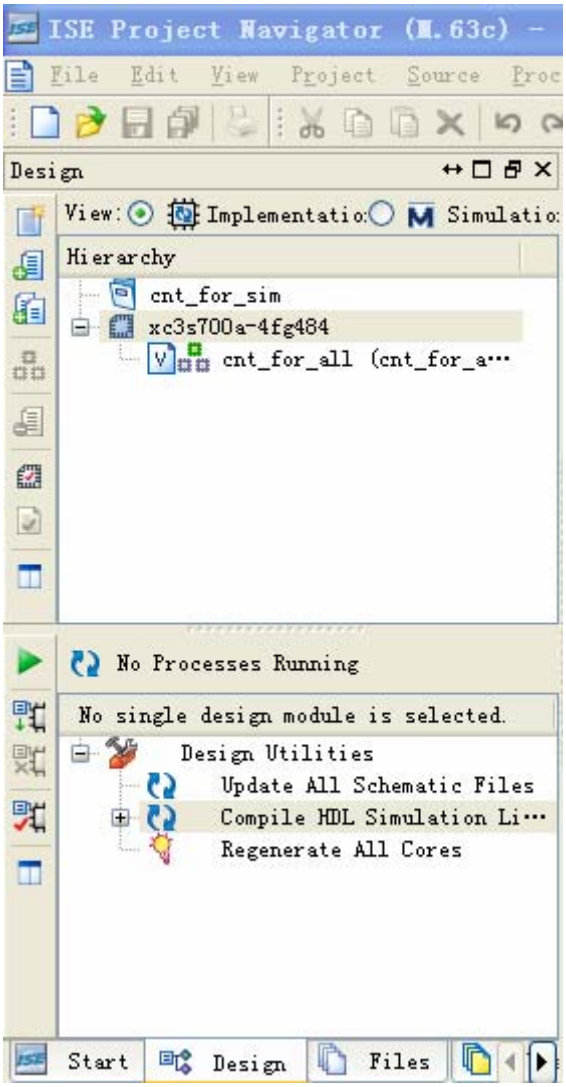
```
clk = 0;
rst_n = 0;

// Wait 100 ns for global reset to finish
#100;

// Add stimulus here
rst_n = 1'b1;
end
always #10 clk = ~clk;
endmodule
```

第七步：编译行为仿真库：

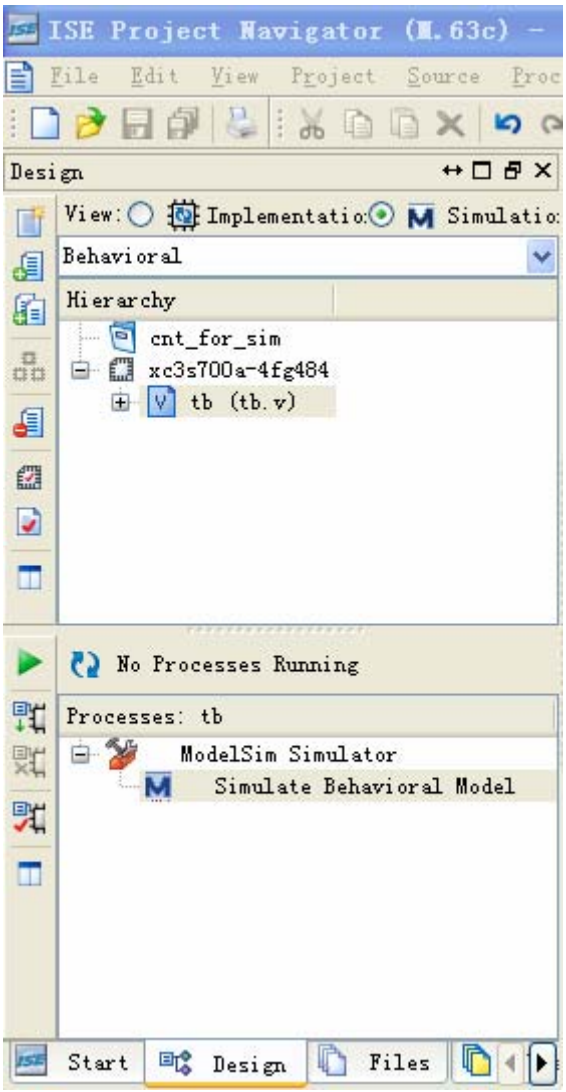
双击 Compile HDL Simulation Library，操作如下图。

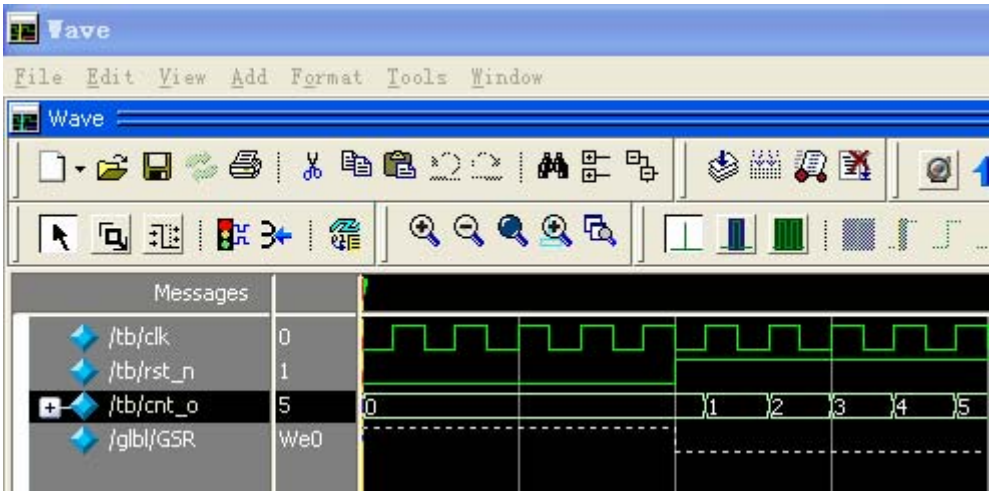


注：此后的任何工程，功能仿真都无需执行这一步了。因为编译的库直接在 ISE 的安装目录里创建。

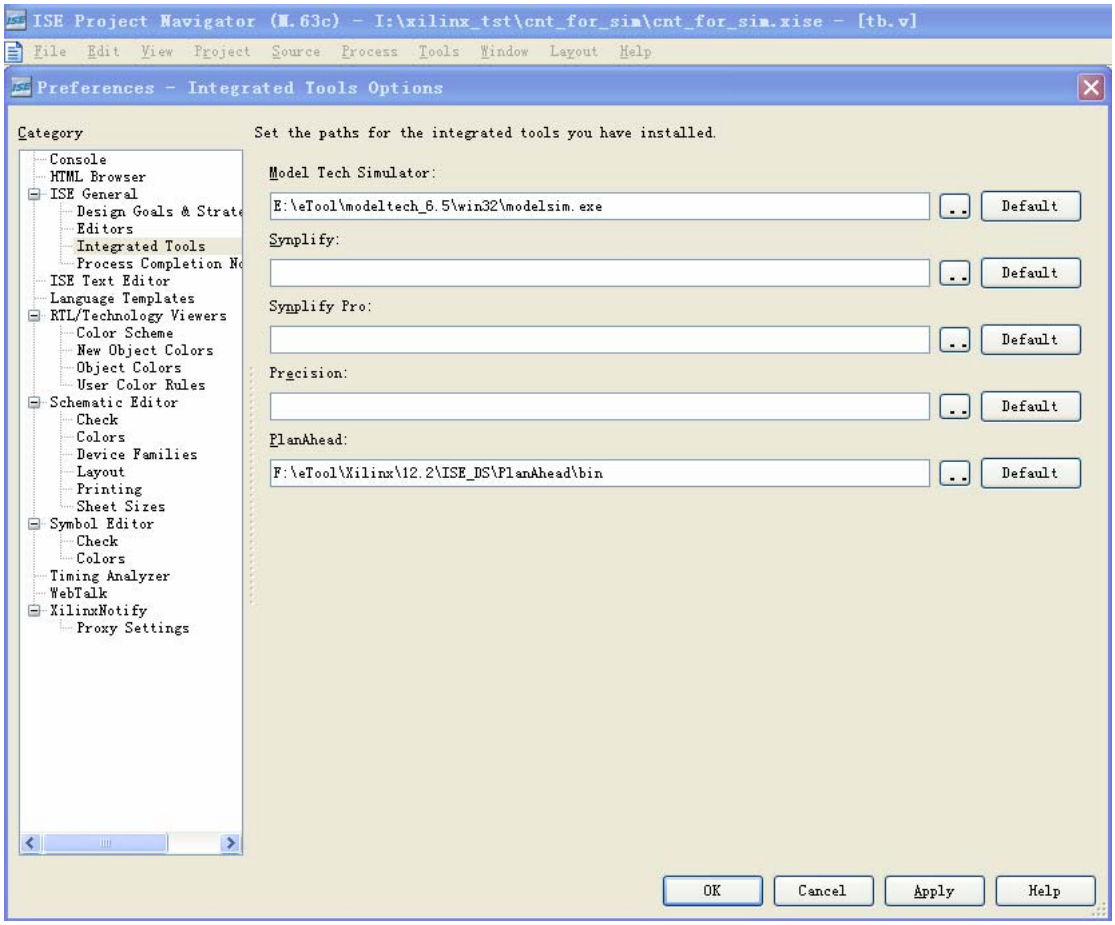
第八步：启动 Modelsim 仿真：

双击 Simulation Behavioral Model，操作如下图。





注意：在 ISE 中调用 Modelsim，需要设置其集成的第三方工具路径。详细操作如下：Edit->Preferences，操作如下图：


ISE Project Navigator (M.63c) - I:\xilinx_tst\cnt_for_sim\cnt_for_sim.xise - [tb.v]
File Edit View Project Source Process Tools Window Layout Help
Preferences - Integrated Tools Options
Category
Console
HTML Browser
ISE General
Design Goals & Strate
Editors
Integrated Tools
Process Completion No
ISE Text Editor
Language Templates
RTL/Technology Viewers
Color Scheme
New Object Colors
Object Colors
User Color Rules
Schematic Editor
Check
Colors
Device Families
Layout
Printing
Sheet Sizes
Symbol Editor
Check
Colors
Timing Analyzer
WebTalk
XilinxNotify
Proxy Settings
Set the paths for the integrated tools you have installed.
Model Tech Simulator:
E:\eTool\modeltech_6.5\win32\modelsim.exe
Default
Synplify:
Default
Synplify Pro:
Default
Precision:
Default
PlanAhead:
F:\eTool\Xilinx\12.2\ISE_DS\PlanAhead\bin
Default
OK
Cancel
Apply
Help