天龙八步 之

Xilinx ISE 12.2 调用 Modelsim 进行行为仿真详解

最近闲来无事,整点东西,以飨各位。

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第一步:新建工程:

File->New Project 创建工程 cnt_for_sim, 操作如下图。

New Project Wiza	nrd	
Create New Project Specify project 1	ocation and type.	
Enter a name, locat	ions, and comment for the project	
N <u>a</u> me:	cnt_for_sim	
Location:	I:\xilinx_tst\cnt_for_sim	
Working Directory:	I:\xilinx_tst\cnt_for_sim	
Description:		
Select the type of	top-level source for the project	
<u>I</u> op-level source ty	pe:	
HDL		
More Info		Next > Cancel

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🚾 New Project Wizard

Project Summary Project Navigator will create a new project with the following specifications. Project: Project Name: cnt_for_sim Project Path: I:\xilinx_tst\cnt_for_sim Working Directory: I:\xilinx_tst\cnt_for_sim Description: Top Level Source Type: HDL Device: Device Family: Spartan3A and Spartan3AN Device: xc3s700a fg484 Package: Speed: -4 Synthesis Tool: XST (VHDL/Verilog) Simulator: Modelsim-SE Mixed Preferred Language: Verilog Property Specification in Project File: Store all values Manual Compile Order: false VHDL Source Analysis Standard: VHDL-93 Message Filtering: disabled More Info < Back Finish Cancel

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第二步:新建文件:

Project->New Source 创建文件 cnt_for_all.v, 操作如下图。

🚾 Hew Source Vizard					×				
Select Source Type Select source type, file name and its location.									
 IP (CORE Generator & Architecture Wizard) Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Package VHDL Test Bench Embedded Processor 	File name: cnt_for_all Location: I:\xilinx_tst\ Mdd to proj	ent_for	r_sim						
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New Source Vizard									
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🚾 New Source Vizard X Summary Project Navigator will create a new skeleton source with the following specifications. Add to Project: Yes Source Directory: I:\xilinx_tst\cnt_for_sim Source Type: Verilog Module Source Name: cnt_for_all.v Module name: cnt_for_all Port Definitions: clk Pin input rst_n Pin input 7:0 cnt o Bus: output More Info < Back Finish Cancel 🖾 ISE Project Navigator (N.63c) - I:\xilinx_tst\cnt_for_sim\cnt_for_sim.xise - [cnt_for_all.v] 📄 File Edit Yiew Project Source Process Tools Mindow Layout Help ↔□♂× € Design 👔 View: 💿 🄯 Implementatio: 🔿 🕅 Simulatio: 🗾 // Company: 3 Hierarchy B // Engineer: 4 - 🔄 cnt_for_sim 11 1 5 5 🖨 🛄 xc3s700a-4fg484 // Create Date: 11:43:33 01/23/2011 6 V cnt_for_all (cnt_for_a... 00 // Design Name: 7 // Module Name: 10 8 cnt_for_all 5 9 // Project Name: 1 10 // Target Devices: 1 // Tool versions: 11 % 1 12 // Description: 3 11 13 // Dependencies: * 14 11 15 // Revision: 🚷 No Processes Running 16 // Revision 0.01 - File Created 17 Processes: cnt_for_all // Additional Comments: 18 5 Design Summary/Reports 19 11 関 • 🏂 Design Utilities 20 咒 Đ User Constraints module cnt_for_all(21 ÷ 🚺 Synthesize - XST input clk, 22 E (2) Implement Design input rst_n, 23 Generate Programming File output [7:0] cnt o (2) 24 🕀 强 Configure Target Device 25 1: Analyze Design Using ChipScope 0 26

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cnt_for_all.v

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第三步:完善 cnt_for_all.v,如下: module cnt_for_all(input clk, input rst_n,

🌌 Start 🖻 Design 🚺 Files 🚺 () 📄

endmodule

第四步:综合文件:

双击 Synthesize – XST,操作如下图。



第五步: 生成 verilog test bench 文件: 右击要仿真的文件 cnt_for_all.v,选择 New Source,操作如下图。

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~	W Verilog Test Fixture	
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	VHDL Library	I:\xilinx_tst\cnt_for_sim
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	🗭 Embedded Processor	
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第六步: 完善 tb.v 文件: 操作如下图:



initial begin // Initialize Inputs clk = 0; rst_n = 0; // Wait 100 ns for global reset to finish #100; // Add stimulus here rst_n = 1'b1; end always #10 clk = ~clk; endmodule

第七步:编译行为仿真库:

双击 Compile HDL Simulation Library,操作如下图。









注意:在 ISE 中调用 Modelsim,需要设置其集成的第三方工具路径。详细操作如下: Edit->Preferences,操作如下图:

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🚾 Preferences - Integr	ated Tools Options	×
Category Console HTML Browser ISE General Design Goals & Strate HTML Browser Integrated Tools Process Completion Ne ISE Text Editor Language Templates RTL/Technology Viewers Object Colors User Color Rules Schematic Editor Colors Device Families Layout Printing Sheet Sizes Symbol Editor Check Colors Timing Analyzer WebTalk XilinxNotify Proxy Settings	Set the paths for the integrated tools you have installed. Model Tech Simulator: E:\eTool\modeltech_6.5\win32\modelsim.exe Symplify: Symplify Fro: Prgcision: PlanAhead: P:\eTool\Xilinx\12.2\ISE_DS\PlanAhead\bin	Default Default Default Default Default Default
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